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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
GARCIA OTERO, EDUARDO

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/360,069	WOHL ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION-Final Action

Introduction

1. Title is: METHOD AND SYSTEM FOR GENERATING AN ATPG MODEL OF A MEMORY FROM BEHAVIORAL DESCRIPTIONS
2. First named Inventor is: WOHL
3. This is a Final Action, in reply to Amendment received 9/16/02.
4. Claims 1-36 have been submitted, examined, and rejected.

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5. **Handbook** refers to CRC Handbook of Mathematical Sciences, 5th Edition, William H. Beyer, CRC Press, Inc., Fourth Printing, 1985, ISBN 0-8493-0655-8, page 47.
6. **Beausang'771** refers to Beausang US Patent 5,696,771.
7. **Cheng** refers to Tutorial and Survey Paper: Gate-Level Test Generation for Sequential Circuits by Kwang-Ting Cheng, ACM Transactions on Design Automation of Electronic Systems, Vol. 1, No. 4, October 1996, Pages 405-442.

AMENDMENT AND RESPONSE-amendments

8. The amendments to the specification, claims, and figures are **accepted as not introducing new matter.**
9. At Amendment Page 3, Applicant does not dispute that Figure 5 illustrates prior art. Applicant has amended Figure 5 to state "(Conventional Art)". The Examiner hereby interprets the phrase "Conventional Art" as satisfying the requirement of designation by a legend such as "Prior Art", as required by MPEP § 608.02(g).

10. In view of said amendments, and in view of Applicant's persuasive assertion at Page 3 that Figure 2 is not prior art, the Examiner **withdraws all the initial objections to the specification and to the drawings.**

new objections-claims

11. There are some inconsistencies between the clean amended Claim 1 on Page 2 and the version with markings on Page 16. For example, clean version states "**and** ATPG", in contrast, the marked version states "**an** ATPG". The marked version appears logically correct, but note that PTO printing is based on the clean copy. Please correct.
12. Further, line 5 of amended Claim 1 states "stored a computer system memory". Apparently this should read "stored in a computer system memory".
13. Claim 1 (amended) states "subset", apparently should read "proper subset".
14. Claim 3 states "said simulation of said memory", apparently should read "said simulation model of said memory".
15. **Thus, the above inconsistencies are hereby objected to.**

AMENDMENT AND RESPONSE-35 USC § 112- first paragraph- enablement

16. At Amendment Page 4, Applicant persuasively asserts that **"predefined subset"** in Claim 1 is enabled. This rejection is withdrawn.
17. At Amendment Page 5, Applicant persuasively asserts that **"excludes timing information"** in Claim 2 is enabled.
18. At Amendment Page 5 and 6, Applicant persuasively asserts that **"excluding physical layout information"** in Claim 3 is enabled.

19. At Amendment Page 12, Applicant persuasively asserts that **"displaying a graphical representation of said primitives"** in Claim 12 is enabled.

20. The above persuasive assertions similarly apply to the dependent claims of said Claims 1, 2, 3, and 12.

21. **Thus, all initial enablement rejections are withdrawn.**

AMENDMENT AND RESPONSE-35 USC § 112- second paragraph- indefinite

22. At Amendment Page 8, Applicant persuasively asserts that **"without physical layout"** in Claim 3 is definite, by distinguishing between physical layout and logical interconnections. This persuasive assertion also applies to the dependent claims.

AMENDMENT AND RESPONSE-35 USC § 112- second paragraph- indefinite-no prior art examination

23. At Amendment Page 9, Applicant persuasively requests examination of Claims 3, 15, and 27 against prior art, stating that they are "enabled and definite for the above-stated reasons".

AMENDMENT AND RESPONSE-lack of utility

24. Applicant's assertion of utility is persuasive.

Claim Interpretation

25. **The claim language is interpreted in light of the specification.** Limitations from the specification must not be imported into the claims, but definitions from the specification must be imported into the claims.

26. Claim 1 (amended) states "subset". This is interpreted as "proper subset". Detailed discussion below.

AMENDMENT AND RESPONSE-Claim Rejections - 35 USC § 102(b) and 103(a)

27. At Amendment Page 9, Applicant asserts that the 86 words (excluding the preamble) of Claim 1 contain 11 elements and 9 functional limitations.

28. Applicant's asserted 11 elements (A1-A11) are:

- A1-a structural model
- **A2-a memory**
- **A3-an automatic test pattern generator (ATPG)**
- **A4-a simulation model**
- A5-a simulation library
- A6-a computer system memory
- A7-a behavioral hardware description language
- A8-a simplified behavioral model
- A9-a predefined subset
- A10-a computer system
- A11-a plurality of ATPG memory primitives.

29. These asserted 11 elements will be considered individually in view of the amended Claim 1 at Page 2-3 of the Amendments. For clarity, the Examiner has added line numbers to the 14 lines of Claim 1. After careful examination, the Examiner finds the following 10 elements (E1-E9). These elements are listed in the order found in the claim.

- **E1-simulation model of a memory**
- E2-simulation library
- E3-computer system memory
- E4-behavioral hardware description language
- E5-simplified behavioral model of said memory
- E6-predefined subset
- E7-computer system

- E8-structural model of said memory
- E9-plurality of ATPG memory primitives.

30. Note that the Applicant lists A2 **"a memory"** as an element. Perhaps it would be more accurate to define this element as E1 "structural model of a memory. Please note the sequence of models in Claim 1: a simulation model of a memory generates a simplified behavioral model of a memory, which translates into a structural model of a memory. The words "a memory" appear ambiguous unless they are identified by a specific model (simulation, simplified behavioral, or structural). Perhaps it is more accurate to view these as models.
31. Further, note that that there is a "computer system memory" in the claim, which adds to the ambiguity. The Applicant lists this as a separate element.
32. There appear to be logical antecedent difficulties with saying "simulation model of said memory" referring back to "structural model of a memory". Note that the structural model of a memory is created after (and based upon) the simulation model of a memory.
33. Note that the Applicant lists **A3 "an automatic test pattern generator"** as an element. This phrase occurs only in the preamble, and appears to be an intended use. It does not appear to be an element of the claim.
34. Applicant lists **A4 "a simulation model"** as an element. It may be more clear to list this as "a simulation model of a memory".
35. To summarize, A2 "a memory" and A3 "an automatic test pattern generator" do not appear to be an elements.
36. Applicant further asserts 9 functional limitations:

- A1-accessing
- A2-wherein said simulation model is described in a behavioral hardware description language
- A3-generating
- A4-re-describing said memory with a predefined subset

- A5-translating
- A6-automatically
- A7-under control
- A8-wherein said structural model comprises a plurality of ATPG memory primitives
- A9-storing.

37. After careful examination, the Examiner finds the following 7 functional limitations. For clarity, the Examiner has made some very slight grammatical corrections as discussed in the above claim objections and claim interpretations:

- E1-**accessing** a simulation model of said memory
- E1-simulation library **stored** in a computer system memory
- E3-simulation model is **described** in a behavioral hardware description language
- E4-**generating** a simplified behavioral model of said memory by re-describing said memory with a predefined subset of said behavioral hardware language.
- E5-**translating, automatically and under control of a computer system,** said simplified behavioral model into said structural model of said memory
- E6-wherein said structural model **comprises** a plurality of ATPG memory primitives
- E7-**storing** said structural model in said computer system memory

38. Note that Applicant's functional limitations A3 "generating" and A4 "re-describing" appear to be the same functional limitation. Note the exact wording in the claim: "generating...by re-describing". It is not clear how these are different.
39. Note that E6 "simulation library stored in a computer system memory" appears to be a functional limitation, but is absent from the Applicant's list.
40. Applicant's highly detailed analysis has been very useful in analyzing the claims.
41. Claim 1 (amended) is a "method" claim, which is clearly divided by semicolons into 4 major process steps: accessing, generating, translating, and storing.

Claim Rejections - 35 USC § 103

42. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

43. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

    1. Determining the scope and contents of the prior art.
    2. Ascertaining the differences between the prior art and the claims at issue.
    3. Resolving the level of ordinary skill in the pertinent art.
    4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

44. Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable.

45. Claim 1 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Beausang US Patent 5,696,771 in view of Legal Precedent (omission of an element and its function) and Cheng.

46. Claim 1 is an independent claim with 4 steps.

47. The first step is **"accessing a simulation model of said memory, from a simulation library stored in a computer system memory, wherein said simulation model is described in a behavioral hardware description language".** This step is disclosed by Beausang '771 at FIG 8 element 605 "HDL DESCRIPTION". Note that HDL stands for "hardware description language". The Examiner hereby takes official notice that it is common knowledge to create simulation models of memories using hardware description languages (such as VHDL or Verilog), and to store these models in a simulation library in a computer system memory, and to access this simulation model.

48. Applicant has the right to traverse this official notice according to MPEP § 2144.03: "if applicant traverses such an assertion, the examiner should cite a reference in support of his or her position". However, please note that MPEP § 2144.03 also states "See also In re Boon, 439 F.2d 724, 169 USPQ 231 (CCPA 1971) (a challenge to the taking of judicial notice must contain adequate information or argument to create *on its face* a reasonable doubt regarding the circumstances justifying the judicial notice)". Specifically, please note that In re Boon states, at 169 USPQ 231, page 234, that "as we held in Ahlert, an applicant must be given the opportunity to challenge either the correctness of the fact asserted or the notoriety or repute of the reference cited in support of the assertion. We did not mean to imply by this statement that a bald challenge, with nothing more would be all that was needed", and "require that a challenge to judicial notice by the board contain adequate information or argument so that on its face it creates a reasonable doubt regarding the circumstances justifying the judicial notice." Additionally, please note that 37 CFR 1.671(c)(3) states "*Judicial notice* means official notice". **Therefore, in view of MPEP § 2144.03 and In re Boon and 37 CFR 1.671(c)(3), the Applicant should note that a mere "bald challenge, with nothing more" to the above official notice will be given very little weight.**

49. The third step is **"translating, automatically and under control of a computer system, said simplified behavioral model into said structural model of said memory, wherein said structural model comprises a plurality of ATPG memory primitives".** This step is disclosed by Beausang '771 at FIG 8 element 655 "ATPG

AND FORMAT", and at Column 14 line 40 "logical primitives". The Examiner hereby takes official notice that "translating, automatically and under control of a computer system" a behavioral model into a structural model is well known in the art.

50. Beausang'771 apparently does not expressly disclose the second and fourth steps.

51. The second step is **"generating a simplified behavioral model of said memory by re-describing said memory with a predefined subset of behavioral hardware description language".** The definition of "subset" is critical. Merriam-Webster's Collegiate Dictionary Tenth Edition defines subset "a set each of whose elements is an element of an inclusive set". CRC Handbook of Mathematical Sciences, 5th Edition, defines subset in the same way, but with much more detail in the section titled "Algebra of Sets". Concept 2 in the Algebra of Sets states: *A* is a subset of set *B* provided *a* is an element of the set *A* implies *a* is an element of the set *B*. Every set has as a subset the empty or null set which has no elements.

52. Thus, the dictionary general definition matches the handbook's mathematical definition. Note that every set is a subset of itself. This point is made clear by distinguishing "subset" from "proper subset". Note that Concept 3 in the Algebra of Sets states: set *A* equals set *B*, if and only if *A* is a subset of *B* and *B* is a subset of *A*. *A* is a proper subset of *B*, if and only if *A* is a subset of *B* and *A* does not equal *B*; then *B* has at least one element which does not belong to *A*.

53. However, based on the context of the claim, and based on the phrase "simplified behavioral model" in the claim, the Examiner believes and interprets that Applicant intended to claim "a predefined proper subset".

54. Legal Precedent. MPEP 2144.04(II) states that "Omission of an Element and Its Function Is Obvious If the Function of the Element Is Not Desired". Here, for example, a subset may be created by eliminating timing information when "not desired or required" according to MPEP 2144.04(II). AS a second example, a second subset may be created by eliminating layout information when "not desired or required" according to MPEP 2144.04(II). Thus, this second step is disclosed by legal precedent.

55. The fourth step is **"storing said structural model in said computer system memory".** The Examiner hereby takes official notice that it is common knowledge in the art to store structural models in computer system memories.

56. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Legal Precedent and Cheng to modify Beausang'771. One of ordinary skill in the art would have been motivated to use a subset (Legal Precedent) create simulation models of memories using hardware description languages (such as VHDL or Verilog) in order to simulate integrated circuits while "ignoring the circuit delays" according to Cheng at Page 407. Further, one of ordinary skill in the art would have been motivated to store these models in a simulation library in a computer system memory in order to easily access these models for various computer simulations to test the circuit design.

57. **Claim 2 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Beausang US Patent 5,696,771 in view of Legal Precedent (omission of an element and its function) and Cheng. Claim 2 depends from Claim 1, with 1 additional limitation.

58. Beausang'771 apparently does not expressly disclose the additional limitation.

59. **"simplified behavioral model excludes timing information"** is disclosed by Legal Precedent, as discussed above in Claim 1 (amended).

60. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Legal Precedent and Cheng to modify Beausang'771. One of ordinary skill in the art would have been motivated to use a subset (Legal Precedent) create simulation models of memories using hardware description languages (such as VHDL or Verilog) in order to simulate integrated circuits while "ignoring the circuit delays" according to Cheng at Page 407 and thus save time. Further, one of ordinary skill in the art would have been motivated to use store these models in a simulation library in a computer system memory in order to easily access these models for various computer simulations to test the circuit design.

61. **Claim 3 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Beausang US Patent 5,696,771 in view of Legal Precedent (omission of an element and its function) and Cheng. Claim 3 depends from Claim 2, with 1 additional limitation.

62. Beausang'771 apparently does not expressly disclose the additional limitation.
63. **"simplified behavioral model excludes physical layout information"** is disclosed by Legal Precedent, as discussed above in Claim 1 (amended). Note that eliminating physical layout information is analogous to eliminating timing information because using simplified models reduces the time required to run simulations, and reduces the computer system memory required to run simulations.
64. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Legal Precedent and Cheng to modify Beausang'771. One of ordinary skill in the art would have been motivated to use a subset (Legal Precedent) create simulation models of memories using hardware description languages (such as VHDL or Verilog) in order to simulate integrated circuits while "ignoring the circuit delays" according to Cheng at Page 407 and thus save time performing simulations. Also, one of ordinary skill in the art would have been motivated to use a subset excluding physical layout information in order to ignore layout and thus save time performing simulations. Further, one of ordinary skill in the art would have been motivated to use store these models in a simulation library in a computer system memory in order to easily access these models for various computer simulations to test the circuit design.
65. **Claims 4-12** all depend from Claim 1, and are rejected for the same reasons as Claim 1, in addition to the reasons previously stated in the previous Office Action, mailed 5/9/02.
66. **Claims 13-24 are "computer readable medium" claims** with the same limitations as Claims 1-12, and therefore are rejected for the same reasons.
67. **Claims 25-36 are "computer controlled electronic design automation systems"** (apparatus) claims with the same limitations as Claims 1-12 and therefore are rejected for the same reasons.

Conclusion

68. Claim 1 (amended) requires numerous small corrections by Applicant, as discussed above in the claim objections and claim interpretation sections.
69. All pending claims are rejected.

Response to Substantial Amendments-FINAL OFFICE ACTION

70. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

71. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

72. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 7:00 PM.

73. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone numbers for this group are:

74. (703) 746-7238 --- for communications after a Final Rejection has been made;

75. (703) 746-7239 --- for other official communications; and

76. (703) 746-7240 --- for non-official or draft communications.

77. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

* * * *

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER